Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): An ESD protection device with complementary dual drain implant comprising:

a) an N-well implanted in a P-substrate;

b) an N+ diffusion implanted on top of said N-well, such that said N+ diffusion extends into said P-substrate on both sides of said N-well;

c) where said N+ diffusion is shared by the drains of two adjacent NMOS transistors;

d) a pad coupled conductively to said N+ diffusion between said drains; and

e) a P-ESD implant interposed between said N+ diffusion and said N-well such that said N-well is electrically coupled to said N+ diffusion, where said P-ESD implant lowers the avalanche voltage of a transistor by reducing the breakdown voltage of the drain/P-substrate junction, and where the implant dosage for said P-ESD implant is less than the implant dosage for said N+ diffusion but higher than the implant dosage for said N-well.

Claim 2 (canceled).

Claim 3 (original): The ESD protection device of claim 1, wherein said P-ESD is electrically coupled to said P-substrate by extending into said P-substrate.

Claim 4 (original): The ESD protection device of claim 1, wherein said drains of said two NMOS transistors are at opposite ends of said N-well.

Claim 5 (original): The ESD protection device of claim 1, wherein said N-well extends in depth beyond the bottom of said P-ESD implant.

Claims 6 – 13 (canceled).

Claim 14 (currently amended): An ESD protection device with complementary dual drain implant comprising:

a) an N-well implanted in a P-substrate;

b) an N+ diffusion implanted on top of said N-well, such that said N+ diffusion extends into said P-substrate on both sides of said N-well;

c) where said N+ diffusion is shared by the drains of two adjacent NMOS transistors;

d) a pad coupled conductively to said N+ diffusion between said drains; and

e) a P-ESD implant interposed between said N+ diffusion and said N-well such that said P-ESD implant is embedded within said N+ diffusion and said N-well, where the P-ESD implant dosage is chosen in such a way as to counterdope said N-well, where said counterdoping creates additional junction areas between said N+ diffusion and said P-ESD implant, and where said additional junction areas participate in the avalanche breakdown.

Claim 15 (canceled).

Claim 16 (original): The ESD protection device of claim 14, wherein where said P-ESD implant lowers the avalanche voltage of a transistor by reducing the breakdown voltage of the drain- P-substrate junction.

Claim 17 (canceled).

Claim 18 (original): The ESD protection device of claim 14, wherein said counterdoping creates additional junction areas on those faces of said P-ESD implant which are in contact with said N-well, where said additional junction areas participate in the avalanche breakdown.

Claim 19 (original): The ESD protection device of claim 14, wherein electrical connections between said P-ESD implant and said P-substrate are provided in surfaces where said P-ESD implant is in contact with said P-substrate.

Claim 20 (original): The ESD protection device of claim 14, wherein said P-ESD implant is interposed between said N+ diffusion and said N-well such that said N-well is electrically coupled to said N+ diffusion.

Claims 21 – 27 (canceled).